

GROOVED HEAT SPREADER FOR STRESS REDUCTION IN IC PACKAGE

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method and package that provides reduced surface and internal stress in the packaging medium.

(2) Description of the Prior Art

Semiconductor devices are typically produced by simultaneously creating a large number of identical integrated circuit (IC) devices (also referred to as semiconductor die or simply as die) in or on the surface of a semiconductor substrate in arrays of rectangular elements. Electrical access is provided to the individual die by providing contact pads, also referred to as Input/Output (I/O) pads, on the surface of the die. The I/O pads are further connected to elements within the die by means of interconnect metal that is used as signal lines, ground planes and power lines.

The process of packaging semiconductor devices typically starts with a leadframe of a substrate that is ceramic or plastic

based, such as Dual-In-Line packages (DIP), Pin Grid Arrays (PGA), Plastic Leaded Chip Carriers (PLCC), Quad Flat Packages (QFP) and Ball Grid Array (BGA) packages.

The Quad Flat Package (QFP) has been created to achieve high pin count integrated packages with various pin configurations. The pin Input/Output (I/O) connections for these packages are typically established by closely spaced leads distributed along the four edges of the flat package. This limits the I/O count of the packages and therefore the usefulness of the QFP. The Ball Grid Array (BGA) package has been created whereby the I/O connects for the package are distributed around the periphery of the package and over the complete bottom of the package. The BGA package can therefore support more I/O points and provides a more desirable package for high circuit density with high I/O count. The BGA contact points are solder balls that in addition facilitate the process of flow soldering of the package onto a printed circuit board. The solder balls can be mounted in an array configuration and can use 40, 50 and 60 mil spacings in a regular or staggered pattern.

Another packaging concept is realized with the use of so-called flip chips. The flip chip is a semiconductor device that has conductive layers formed on its top surface. The top surface

of the flip chip is further provided with so-called solder bumps. At the time of assembly of the flip chip, the chip is turned over (flipped over) so that the solder bumps are now facing downwards and toward the circuit board, typically a printed circuit board, on which the flip chip is to be mounted.

The invention addresses the aspect of a semiconductor device package that contains a heat spreader, the design of the heat spreader of the invention is such that stress is significantly reduced in surfaces of the package.

US 5,905,633 (Shirn et al.) shows a heat spreader with grooves 68.

US 6,158,502 (Thomas) shows a heat spreader with grooves, this reference differs from the invention.

US 6,117,352 (Weaver et al. shows an etched heat spreader.

US 6,011,304 (Mertol), US 5,949,137 (Dornadia et al.), US 5,484,959 (Burns) show related heat spreaders.

SUMMARY OF THE INVENTION

A principle objective of the invention is to provide a semiconductor device package comprising a heat spreader, whereby the design of the heat spreader is such that stress is significantly reduced in surfaces of the package.

In accordance with the objectives of the invention a new design is provided for the heat spreader of a semiconductor package. Grooves are provided in a surface of the heat spreader, subdividing the heat spreader for purposes of stress distribution into multiple sections. This division of the heat spreader results in a reduction of the mechanical and thermal stress that is introduced by the heat spreader into the device package. Mechanical and thermal stress, using conventional heat spreader designs, has a negative, stress induced effect on the semiconductor die, on the contact points (bump joints) of the semiconductor die and on the solder ball connections of the package.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a cross section of a first prior art semiconductor package.

Fig. 2 shows a cross section of a second prior art semiconductor package.

Figs. 3a through 3c show simplified cross sections and the heat spreader of a third prior art semiconductor package, this package best compares with the package of the invention, as follows:

Fig. 3a shows a cross section where the semiconductor die is mounted on the surface of a PCB,

Fig. 3b shows a cross section after the stiffener and a heat spreader have been attached,

Fig. 3c shows a bottom view of the heat spreader.

Figs. 4a and 4b show cross sections of the package of the invention, Figs. 4c and 4d show top views of the heat spreader of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows a cross section of a prior art package. The elements that are highlighted in Fig. 1 are the following:

- 10, a Printed Circuit Board (PCB) on the surface of which a semiconductor die is mounted
- 12, a semiconductor die
- 14, a layer of metal traces (interconnect lines) that is used for interconnect distribution
- 16, a solder resist layer that protects the surface of the layer 14 of interconnect traces
- 18, a dielectric interconnect substrate containing interconnect traces; an opening has been created in the interconnect substrate, the die 12 is placed inside this opening; this interconnect substrate can take forms others than the form that is shown in cross section in Fig. 1 such as single strips and the like; the number of layers of interconnect traces contained within the interconnect substrate is also not determinate
- 19, bond wires that connect contact points (not shown) on the top surface of die 12 with contact points (not shown) that have been provided in the top surface of the interconnect substrate 18
- 20, an encapsulant the encapsulates die 12, the interconnects 19 and the interconnect substrate 18
- 21, an (symbolic and representative) interconnect between contact points (not shown) on the top surface of interconnect substrate 18 and contact points (not shown) on the bottom surface of the interconnect substrate 18

09012739.072601

- 22, a layer of interconnect traces that is provided over the bottom surface of PCB 10
- 24, a solder mask overlying the interconnect traces 22, openings have been created in the solder mask 24 which expose points of electrical contact (not shown) of the interconnect traces 22
- 26, contact balls that have been inserted into the solder mask 22 and that make electrical contact with points of contact (not shown) of the interconnect traces 22.

Fig. 2 shows a cross section of a second prior art semiconductor package, this cross section is based on US Patent 5,905,633 (Shim et al.) and is introduced in order to (at a later time) highlight differences between the instant invention and the Shim et al. invention.

While element 10 has been described above as being a Printed Circuit Board, it must be realized that this element is not limited to being a Printed circuit Board but can be a flex circuit or a metallized or glass substrate or semiconductor device mounting support.

Highlighted in cross section shown in Fig. 2 are the following elements of the semiconductor package:

- 10, a Printed Circuit Board (PCB) on the surface of which a semiconductor die is mounted
- 12, a semiconductor die
- 14, a layer of metal traces (interconnect lines) that is used for interconnect distribution
- 16, a solder resist layer that protects the surface of the layer 14 of interconnect traces
- 19, bond wires that connect contact points on the top surface of die 12 with contact points that have been provided in the top surface of the interconnect traces 14
- 20, an encapsulant the encapsulates die 12
- 22, a layer of interconnect traces the is provided over the bottom surface of PCB 10
- 24, a solder mask overlying the interconnect traces 22, openings have been created in the solder mask 24 which expose points of electrical contact (not shown) of the interconnect traces 22
- 26, contact balls that have been inserted into the solder mask 22 and that make electrical contact with points of contact (not shown) of the interconnect traces 22
- 28, a bonding agent that has been deposited over the surface of layer 16 of solder resist; this bonding mask forms the interconnection between the solder resist 16 and the overlying carrier/heat spreader 30

- 30, the heat spreader of the package; this element is also referred to as a PCB carrier which refers to the method that is used to assembly (multiple) packages of which one is shown in cross section in Fig. 2
- 32, a protective layer, typically comprising, according to Shim et al., silver, nickel or paladium; this layer is to prevent oxidation and corrosion of the metal carrier 30
- 34, grooves that are formed in a surface of the metal carrier 30; these grooves have, according to Shim et al., preferably a V-shaped cross section.

It must be noted from the cross section that is shown in Fig. 2 that the heat spreader (heat sink) 30 is directly attached to the package PCB 10, with intervening layers 14, 16 and 28. Furthermore, the heat sink 30 surrounds the wire bond die 12 and is partially covered by molding compound 20. The functions of grooves 34, Fig. 2, is to provide improved adhesion between the mold compound 20 and the underlying layer 28 of bonding agent by means of improved mechanical interlocking and by extending the moisture penetration path, enhancing the package reliability.

Referring now specifically to the Figs. 3a through 3c, Fig. 3a shows the following prior art elements:

- 10, a substrate such as a PCB on the surface of which a semiconductor die is mounted
- 12, a semiconductor die
- 11, solder bumps that have been provided on a surface of die 12 for electrical interconnection of die 12
- 13, underfill that has been inserted underneath the die 12 and that surrounds the solder bumps 11, and
- 26, contact balls.

Fig. 3b shows in cross section, in addition to the elements that have already been highlighted under the cross section of Fig. 3a, the following prior art elements:

- 15, layers of adhesive that have been deposited over the surface of substrate 10, over the surface of stiffeners 23 and over the surface of semiconductor die 12
- 23, stiffeners of the package
- 25, the heat spreader of the package.

Fig. 3c shows a bottom view of the heat spreader of the package. This bottom surface of the heat spreader that is shown in top view in Fig. 3c is the surface that interfaces with the adhesive layer 15 that has been deposited over the surface of substrate 10, over the surface of stiffeners 25 and over the

surface of semiconductor die 12, this surface therefore faces semiconductor die 12.

For the cross sections that are shown in Figs. 3a through 3c, that is a typical flip-chip BGA (FC-BGA) package, the IC chip 12 is electrically connected with package substrate 10 by solder bumps 11. The underfill 13 (Fig. 3a) is applied, which fills the gap between chip 12 and the substrate 10 and is cured at temperature above room temperature to increase the bump-joint reliability.

In order to meet demands of thermal performance of a high performance IC package, the stiffener 23 (Fig. 3b) and heat spreader 25 (Fig. 3b) are attached as shown in cross section in Fig. 3b. The stiffener 23 is a plain metal plate with a proper opening in the center to allow chip placement and to provide support for the heat spreader attachment. The heat spreader 25 is a plain metal plate, Fig. 3c, and provides heat dissipation for the die 12. The disadvantages of the implementation of the heat spreader as shown in Figs. 3a and 3b is that thermal and mechanical stresses are increased in the die 12, in solder bump 11 points of contact and in the points of contact of contact balls 26. These stresses have a negative effect on the package

integrity and degrade bump-joint reliability. The invention addresses these problems.

Referring now specifically to Figs. 4a through 4d, Fig. 4a shows in cross section the package of the invention with heat spreader 40 in which grooves 42 have been provided. The grooves divide the heat spreader 40 into a number of sections, determined by the number of grooves that are provided in a surface of heat spreader 40. For the example of heat spreader 40 that is shown in top view in Fig. 4c, two grooves 42 are provided dividing the heat spreader into four sections. For the example of heat spreader 44 that is shown in top view in Fig. 4d, four grooves 46 are provided dividing the heat spreader into nine sections. This dividing of the heat spreader results in the separate sections of the heat spreader functioning in almost independent manner whereby the typical stresses that occur in the surface of the heat spreader are now diverted to the (regions of) the grooves. In concentrating thermal and mechanical stresses from across the surface of the heat spreader to the regions of the grooves of the heat spreader, these stresses are greatly reduced in the surface of the semiconductor die 12, the solder bumps 11 and the contact balls 26. This placement of the stress in the regions of the grooves results in enhanced reliability performance of the semiconductor die 12 and the underlying substrate 10 on which the

die is mounted. In addition, thermal and mechanical stress will be reduced on points of electrical contact that are used to interconnect die 12 such as the solder bumps 11 and the contact balls 26. Since the number of grooves that is provided in the surface of the heat spreader is limited, no significant amount of material of the heat sink is removed which results in little or no negative impact on the thermal performance of the package.

Grooves 42 and 46 can be created using methods of etching, machining or punching of the surface of the heat spreader.

To summarize the heat shield of the invention:

- the heat spreader of the semiconductor device package is provided with grooves in the surface that faces the semiconductor die to which the heat spreader is attached
- the location of the grooves that are provided in a surface of the heat spreader is selected such that an optimum level of stress concentration is provided in the regions of the grooves, thus providing stress relieve across the surface of the heat spreader
- the heat spreader of the invention provides a method for concentrating thermal and mechanical stress into well defined regions of the heat spreader; thermal and mechanical stress in prior art heat spreaders is typically present uniformly distributed across the largest surface of a heat spreader and

as such exerts stress across the largest surface of the die to which the heat spreader is attached, and

- the heat spreader of the invention can be provided with one or more grooves, preferably two or four perpendicularly intersecting grooves that divide the surface of the heat spreader in which the grooves have been provided in equal segments.

Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. It is therefore intended to include within the invention all such variations and modifications which fall within the scope of the appended claims and equivalents thereof.

09912739-072601